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10/733,402	12/12/2003	Hong Chul Kim	049128-5136	9110

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,402	KIM, HONG CHUL	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 13, paragraph [0040], line 1 states: "Since the desired leakage current **dose** not flow..." This should be changed to: "Since the desired leakage current **does** not flow...".

Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-30 are provisionally rejected on the ground of nonstatutory double patenting over claims 1-14 of copending Application No. 10/608,187. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows:

The following is an example for comparing claim 22 of this application and claim 13 of copending Application No. 10/608,187.

Claim 22 of this application	Claim 13 of copending Application No. 10/608,187
A ferroelectric liquid crystal display, comprising:	A ferroelectric liquid crystal display device, comprising:
a liquid crystal panel having ferroelectric liquid crystal cells; **data lines** and **gate lines**; **thin film transistors** for supplying voltage on the data lines to the liquid crystal cells in response to a scan voltage on the gate line;	a liquid crystal panel having a plurality of **data and gate lines** and a plurality **of thin film transistors** arranged a first direction in an offset configuration between adjacent data lines;
a **gate driver** for **supplying** a first a **voltage below threshold voltage of the thin film transistor to the gate lines**; and	a **gate driving circuit** for **supplying a voltage below a threshold voltage of the thin film transistors to the gate lines** during an electric field alignment of ferroelectric liquid crystal material of the display device; and
a **data driver** for **supplying** a second	a **data driving circuit** for **controlling**

voltage for electric field alignment to the data lines during electric field alignment of the liquid crystal cell.	opposite polarity **voltages supplied to the adjacent data lines during the electric field alignment** while marinating a voltage supplied to a ferroelectric liquid crystal cell during the electric field alignment.

As shown by the comparison above, claim 22 of the current application is merely a broader version of claim 13 of copending Application No. 10/608,187. The only differences between the claims is the wording used and the addition of the limitation in claim 13 of the copending application that the data driving circuit controls *opposite polarity* voltages while *maintaining a voltage supplied to a ferroelectric liquid crystal cell during the electric field alignment*, however, since the present claim 22 is in comprising format which includes any unclaimed features therefore, the present claims are not patentably distinct from the copending claims.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 14 recites the limitation "the voltage of mutually contrary polarity." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1, 3-9, 11-16, 18-22, 24, 26-27 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US 2003/0067579).

Regarding claim 1, Inoue et al. disclose an electric field alignment method of liquid crystal display (Abstract), comprising the steps of:

applying a first voltage to a gate terminal of a thin film transistor for driving a liquid crystal cell having ferroelectric liquid crystal, wherein the first voltage is below a threshold voltage of the thin film transistor (Paragraph [0178] explains that the gate line is floating meaning that a voltage is applied but the voltage is not enough to turn the transistor ON. Paragraph [0270] explains this method can be used with a ferroelectric liquid crystal panel that needs treatment for alignment. Paragraph [0180] also explains that 5 volts could be applied to the gate lines.); and

supplying a second voltage for electric field alignment of the ferroelectric liquid crystal to the liquid crystal cell (Paragraph [0180] explains that 5 volts is applied to the data line during the time in which the gate line is in the floating state, which is also 5 volts, the that this voltage is applied to the liquid crystal.).

Although Inoue et al. does not explicitly say that leakage current is generated due to the first voltage and that this leakage current is what causes the alignment, the examiner understands that if the gate line is in the floating state, i.e. the transistor is turned OFF but voltage is applied to it, then the voltage applied from the data lines to the source, which is 5 volts, will not pass through the transistor but instead current will leak from the transistor since the transistor is also receiving voltage at the gate from the gate line. This means that the current able to leak through the drain of the transistor is a leakage current and this creates the voltage which is applied to the liquid crystal for alignment. Therefore, the voltages applied to the gate and data lines as taught by Inoue et al. cause a leakage current on the transistor, and thus the liquid crystal molecules are aligned.

Regarding claim 3, Inoue et al. disclose the method according to claim 1, wherein the first voltage is between about –5 volts to about 20 volts (Paragraph [0180] explains that the voltage applied to the gate lines is 5 volts, which is between –5 and 20.).

Regarding claim 4, Inoue et al. disclose the method according to claim 1.

Although Inoue et al. fail to explicitly teach wherein the first voltage is between about 0 volt to 1 volt, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to do so since Inoue et a. already teaches of a voltage within the range of –5 to 20 as claimed in claim 3, which is 5 volts, and also teaches that the gate lines are in a floating state. Therefore making the range between 0 and 1 is only a matter of design choice.

Regarding claim 5, Inoue et al. disclose the method according to claim 1, wherein the first voltage is floating (Paragraph [0178]).

Regarding claim 6, Inoue et al. disclose the method according to claim 1, wherein the second voltage has uniformly maintained polarity and is applied to a source terminal of the thin film transistor such that the second voltage is supplied from the source terminal to a pixel electrode of the liquid crystal cell via leakage current of the thin film transistor to a drain terminal of the thin film transistor that is connected to the

pixel electrode (As explained in the rejection of claim 1, if the gate line is in the floating state, i.e. the transistor is turned OFF but voltage is applied to it, then the voltage applied from the data lines to the source, which is 5 volts, will not pass through the transistor but instead current will leak from the transistor since the transistor is also receiving voltage at the gate from the gate line. This means that the current able to leak through the drain of the transistor is a leakage current and this creates the voltage which is applied to the liquid crystal for alignment. Therefore, the voltages applied to the gate and data lines as taught by Inoue et al. cause a leakage current on the transistor, and thus the liquid crystal molecules are aligned. And as explained in paragraph [0180] the polarity of 5 volts is maintained during the alignment.)

Regarding claim 7, Inoue et al. disclose an electric field alignment method of ferroelectric liquid crystal display having ferroelectric liquid crystal cells in which a thin film transistor is formed at crossings of data lines and gate lines (Figure 6), comprising the steps of:

supplying a first voltage below a threshold voltage of the thin film transistor to the gate lines (Paragraph [0178] explains that the gate line is floating meaning that a voltage is applied but the voltage is not enough to turn the transistor ON. Paragraph [0270] explains this method can be used with a ferroelectric liquid crystal panel that needs treatment for alignment. Paragraph [0180] also explains that 5 volts could be applied to the gate lines.);

supplying a second voltage to the data lines for electric field alignment of the ferroelectric liquid crystal by using leakage current flowing in the thin film transistor (Paragraph [0180] explains that 5 volts is applied to the data line during the time in which the gate line is in the floating state, which is also 5 volts, the that this voltage is applied to the liquid crystal.).

Although Inoue et al. does not explicitly say that leakage current is generated due to the first voltage and that this leakage current is what causes the alignment, the examiner understands that if the gate line is in the floating state, i.e. the transistor is turned OFF but voltage is applied to it, then the voltage applied from the data lines to the source, which is 5 volts, will not pass through the transistor but instead current will leak from the transistor since the transistor is also receiving voltage at the gate from the gate line. This means that the current able to leak through the drain of the transistor is a leakage current and this creates the voltage which is applied to the liquid crystal for alignment. Therefore, the voltages applied to the gate and data lines as taught by Inoue et al. cause a leakage current on the transistor, and thus the liquid crystal molecules are aligned.

Regarding claim 8, Inoue et al. disclose the method according to claim 7, further comprising the step of:

supplying video data to the data lines during normal driving of the liquid crystal display (Paragraph [0166] explains that during normal writing the data bus line writes a voltage to the pixel electrode, i.e. video data is supplied to the lines.).

Regarding claim 9, Inoue et al. disclose the method according to claim 7, further comprising the step of:

supplying scan voltage set to more than the threshold voltage of the thin film transistor to the gate lines during normal driving of the liquid crystal display (Paragraph [0166] explains that during normal writing the gate bus line acts as a switch for supplying the video data, meaning that the gate voltage applied turns On the transistor to allow the data voltage to pass.).

Regarding claim 11, this claim is rejected under the same rationale as clam 3.

Regarding claim 12, this claim is rejected under the same rationale as clam 4.

Regarding claim 13, this claim is rejected under the same rationale as clam 5.

Regarding claim 14, Inoue et al. disclose the method according to claim 7, wherein the voltage of mutually contrary polarity is applied to the data lines (Paragraph [0180] explains that 5 volts are applied to the data lines and this voltage is mutually contrary in polarity to a negative voltage.).

Regarding claim 15, Inoue et al. disclose the method according to claim 14, wherein the polarity of voltage supplied to each of the data lines is uniformly maintained during electric field alignment of the ferroelectric liquid crystal cells (paragraph [0180] explains that 5 volts is applied to each data line meaning that the polarity of uniformly maintained.).

Regarding claim 16, Inoue et al. disclose a liquid crystal display (Figure 6), comprising:

a plurality of ferroelectric liquid crystal cells (Figure 6 and paragraph [0270]);

a plurality of thin film transistors for driving each of the plurality of ferroelectric liquid crystal cells (Figure 6 shows transistors at each cell as explained in paragraph [0178].); and

an electric field alignment circuit for applying a first voltage below a threshold voltage of the thin film transistor to a gate terminal of the thin film transistor and for aligning the plurality of ferroelectric liquid crystal cells under an electric field by using leakage current of the thin film transistor (Paragraph [0178] explains that the gate line is floating meaning that a voltage is applied but the voltage is not enough to turn the transistor ON. Paragraph [0270] explains this method can be used with a ferroelectric liquid crystal panel that needs treatment for alignment. Paragraph [0180] also explains that 5 volts could be applied to the gate lines.).

Although Inoue et al. does not explicitly say that leakage current is generated due to the first voltage and that this leakage current is what causes the alignment, the examiner understands that if the gate line is in the floating state, i.e. the transistor is turned OFF but voltage is applied to it, then the voltage applied from the data lines to the source, which is 5 volts, will not pass through the transistor but instead current will leak from the transistor since the transistor is also receiving voltage at the gate from the gate line. This means that the current able to leak through the drain of the transistor is a leakage current and this creates the voltage which is applied to the liquid crystal for alignment. Therefore, the voltages applied to the gate and data lines as taught by Inoue et al. cause a leakage current on the transistor, and thus the liquid crystal molecules are aligned.

Regarding claim 18, this claim is rejected under the same rationale as claim 3.

Regarding claim 19, this claim is rejected under the same rationale as claim 4.

Regarding claim 20, this claim is rejected under the same rationale as claim 5.

Regarding claim 21, this claim is rejected under the same rationale as claim 6.

Regarding claim 22, Inoue et al. disclose a ferroelectric liquid crystal display, comprising:

a liquid crystal panel having ferroelectric liquid crystal cells (Figure 6 and paragraph [0270]);

data lines and gate lines (Figure 6);

thin film transistors for supplying voltage on the data lines to the liquid crystal cells in response to a scan voltage on the gate line (Figure 6 shows transistors at each cell as explained in paragraph [0178].);

a gate driver for supplying a first a voltage below threshold voltage of the thin film transistor to the gate lines(Paragraph [0178] explains that the gate line is floating meaning that a voltage is applied but the voltage is not enough to turn the transistor ON. Paragraph [0270] explains this method can be used with a ferroelectric liquid crystal panel that needs treatment for alignment. Paragraph [0180] also explains that 5 volts could be applied to the gate lines. Also the examiner interprets that if a voltage is able to be applied to the lines then there would need to be a driver to do so.); and

a data driver for supplying a second voltage for electric field alignment to the data lines during electric field alignment of the liquid crystal cell (Paragraph [0180] explains that 5 volts is applied to the data line during the time in which the gate line is in the floating state, which is also 5 volts, the that this voltage is applied to the liquid crystal. Also the examiner interprets that if a voltage is able to be applied to the lines then there would need to be a driver to do so.).

Although Inoue et al. does not explicitly say that leakage current is generated due to the first voltage and that this leakage current is what causes the alignment, the examiner understands that if the gate line is in the floating state, i.e. the transistor is

turned OFF but voltage is applied to it, then the voltage applied from the data lines to the source, which is 5 volts, will not pass through the transistor but instead current will leak from the transistor since the transistor is also receiving voltage at the gate from the gate line. This means that the current able to leak through the drain of the transistor is a leakage current and this creates the voltage which is applied to the liquid crystal for alignment. Therefore, the voltages applied to the gate and data lines as taught by Inoue et al. cause a leakage current on the transistor, and thus the liquid crystal molecules are aligned.

Regarding claim 24, this claim is rejected under the same rationale as claim 9.

Regarding claim 26, this claim is rejected under the same rationale as claim 3.

Regarding claim 27, this claim is rejected under the same rationale as claim 4.

Regarding claim 29, this claim is rejected under the same rationale as claim 15.

Regarding claim 30, this claim is rejected under the same rationale as claim 5.

9. Claims 2, 10, 17 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US 2003/0067579) in view of APA (Figures 1-5 and page 2, paragraph [0003] to page 9, paragraph [0018] of the specification.).

Regarding claim 2, Inoue et al. disclose the method according to claim 1.

Inoue et al. fail to teach wherein the liquid crystal cell is a Half V-Switching mode ferroelectric liquid crystal cell.

APA discloses wherein a liquid crystal cell is a Half V-Switching mode ferroelectric liquid crystal cell (Paragraph [0012]).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the ferroelectric liquid crystal cells taught by Inoue et al. into a Half V-Switching mode ferroelectric liquid crystal cell as taught by APA in order to have the advantage of high-speed response and wide viewing angle.

Regarding claim 10, this claim is rejected under the same rationale as clam 2.

Regarding claim 17, this claim is rejected under the same rationale as claim 2.

Regarding claim 25, this claim is rejected under the same rationale as claim 2.

10. Claims 23 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US 2003/0067579) in view of Youn (US 2002/0089485).

Regarding claim 23, Inoue et al. disclose the ferroelectric liquid crystal display according to claim 22.

Inoue et al. fail to teach wherein the data driver supplies video data to the data lines by column inversion method during normal driving of the liquid crystal display.

Youn discloses of a liquid crystal device wherein a data driver supplies video data to data lines by a column inversion method during normal driving of the liquid crystal display (Paragraphs [0010]-[0011] explains that the signal voltage is inverted on a column-by-column basis.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the column inversion driving method taught by Youn in the liquid crystal device taught by Inoue et al. in order to correct the problematic characteristic of the liquid crystal material that the liquid crystal material is degraded under the electric field continuously supplied in one direction.

Regarding claim 28, Inoue et al. disclose the ferroelectric liquid crystal display according to claim 22.

Youn discloses of a liquid crystal device wherein a data driver supplies video data to data lines by a column inversion method during normal driving of the liquid crystal display (Paragraphs [0010]-[0011] explains that the signal voltage is inverted on a column-by-column basis.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the column inversion driving method taught by Youn in the liquid crystal device taught by Inoue et al. in order to correct the problematic

characteristic of the liquid crystal material that the liquid crystal material is degraded under the electric field continuously supplied in one direction.

Inoue et al. and Youn fail to teach that the column inversion method is applied during electric field alignment of the ferroelectric liquid crystal, however, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to also use the column inversion method during electric field alignment in order to correct the problematic characteristic of the liquid crystal material that the liquid crystal material is degraded under the electric field continuously supplied in one direction.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

11 October 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER